Extracting Reusable Software Architectures: A Slicing-Based Approach

Jianjun Zhao
Department of Computer Science and Engineering
Fukuoka Institute of Technology
3-10-1 Wajiro-Higashi, Higashi-ku, Fukuoka 811-0295, Japan
Email: zhao@cs.fit.ac.jp

Abstract

An alternative approach to developing reusable components from scratch is to recover them from existing systems. Although numerous techniques have been proposed to recover reusable components from existing systems, most have focused on implementation code, rather than software architecture. In this paper, we apply architectural slicing to extract reusable architectures from existing architectural specifications. Architectural slicing is designed to operate on the architectural specification of a software system to provide knowledge about the high-level structure of a software system, rather than the traditional program slicing which is designed to operate on the source code of a program to provide the low-level implementation details of a program.

1 Introduction

Software architecture is receiving increasingly attention as a critical design level for software systems [17]. The software architecture of a system defines its high-level structure, exposing its gross organization as a collection of interacting components. A well-defined architecture allows an engineer to reason about system properties at a high level of abstraction. Architectural description languages (ADLs) are formal languages that can be used to represent the architecture of a software system. They focus on the high-level structure of the overall application rather than the implementation details of any specific source module. Recently, a number of architectural description languages have been proposed such as WRIGHT[1], Rapide [12], UniCon [16], and ACME [7] to support formal representation and reasoning of software architectures. As software architecture design resources (in the form of architectural specifications) are going to be accumulated, the development of techniques to support software reuse at the architectural level will become an important issue.

One way to support software reuse is to use slicing technique. Program slicing, originally introduced by Weiser [19], is a decomposition technique which extracts program elements related to a particular computation. A *program slice* consists of those parts of a program that may directly or indirectly affect the values computed at some program point of interest, referred to as a *slicing criterion*. The task to compute program slices is called *program slicing*. To understand the basic idea of program slicing, consider a simple example in Figure 1 which shows: (a) a program fragment and (b) its slice with respect to the slice criterion (`Total`,14). The slice consists of only those statements in the program that might affect the value of variable `Total` at line 14. The lines represented by small rectangles are statements that have been sliced away.

Traditional slicing has been studied primarily in the context of conventional programming languages. In such languages, slicing is typically performed by using a control flow graph or a dependence graph [5, 15, 20]. Traditional slicing has many applications in software engineering activities including program understanding [4], debugging, testing, maintenance [6], reuse [3, 11], reverse engineering [2], and complexity measurement [15].

However, existing slicing-based approaches to extract reusable components from existing software systems have mainly focused on the statement level [3, 11], rather than the architectural level. We believe that applying slicing technique to support system reuse at the architectural level promises benefit for software architectural reuse, because while reuse of code is important, in order to make truly large gains in productivity and quality, reuse of software designs and patterns may offer the greater potential for return on investment. By slicing a software architecture, a system designer can extract reusable architectures from it, and reuse them into new system designs for which they are appropriate.

In this paper, we apply architectural slicing to extract reusable architectures from existing architectural specifications. Abstractly, our architectural slicing algorithm takes as input a formal architectural specification (written in its associated architectural description language) of a software system, then it removes from the specification those components and interconnections between components which are not interested by the architect. The rest of the specification, i.e., its architectural slice, can thus be used by the architect in a new system architecture design. This benefit allows one to rapidly reuse existing architecture design resources when performed architecture design.

The primary idea of architectural slicing technique

```
(a) A program fragment.
 1   begin
 2     read(X,Y);
 3     Total := 0.0;
 4     Sum := 0.0;
 5     if X <= 1 then
 6        Sum := Y;
 7        else
 8            begin
 9              read(Z);
10              Total := X * Y;
11            end;
12     end if
13     Write(Total, sum);
14   end
```

```
(b) a slice of (a) on the criterion (Total,14).
 1   begin
 2     read(X,Y);
 3     Total := 0.0;
 4     ▭
 5     if X <= 1 then
 6        ▭
 7        else
 8            begin
 9              ▭
10              Total := X * Y;
11            end;
12     end if
13     ▭
14   end
```

Figure 1: A program fragment and its slice on criterion (`Total`,14).

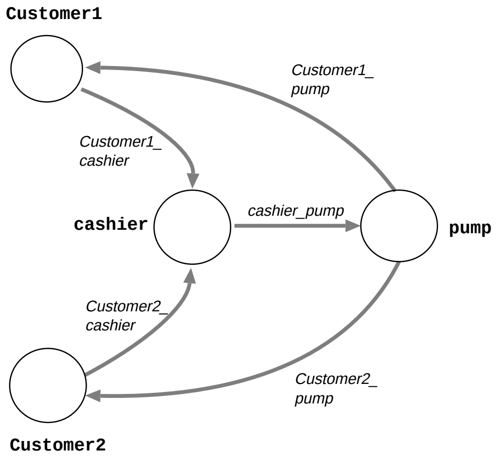

Figure 3: The architecture of the Gas Station system.

has been presented in [20, 21], and this article can be regarded as an outgrowth of our previous work for applying this technique to software architectural reuse. Moreover, the goal of this paper is to provide a sound and formal basis to our slicing-based architectural extraction approach before applying it to real software architecture design.

The rest of the paper is organized as follows. Section 2 briefly introduces how to represent a software architecture using Wright: an architectural description language. Section 3 shows a motivation example. Section 4 defines some notions about slicing software architectures. Section 5 presents the architecture information flow graph for software architectures . Section 6 gives a two-phase algorithm for computing an architectural slice. Concluding remarks are given in Section 7.

2 Software Architectural Specification in Wright

We assume that readers are familiar with the basic concepts of software architecture and architectural description language, and in this paper, we use Wright architectural description language [1] as our target language for formally representing software architectures. The selection of Wright is based on that it supports to represent not only the architectural structure but also the architectural behavior of a software architecture.

Below, we use a simple Wright architectural specification taken from [14] as a sample to briefly introduce how to use Wright to represent a software architecture. The specification is showed in Figure 2 which models the system architecture of a Gas Station system [9].

2.1 Representing Architectural Structure

Wright uses a *configuration* to describe architectural structure as graph of components and connectors.

Components are computation units in the system. In Wright, each component has an *interface* defined by a set of *ports*. Each port identifies a point of interaction between the component and its environment.

Connectors are patterns of interaction between components. In Wright, each connector has an *interface* defined by a set of *roles*. Each role defines a participant of the interaction represented by the connector.

A Wright architectural specification of a system is defined by a set of component and connector type definitions, a set of instantiations of specific objects of these types, and a set of *attachments*. Attachments specify which components are linked to which connectors.

For example, in Figure 2 there are three component type definitions, `Customer`, `Cashier` and `Pump`, and three connector type definitions, `Customer_Cashier`, `Customer_Pump` and `Cashier_Pump`. The configuration is composed of a set of instances and a set of attachments to specify the architectural structure of the system.

2.2 Representing Architectural Behavior

Wright models architectural behavior according to the significant events that take place in the computation of components, and the interactions between components as described by the connectors. The notation for specifying event-based behavior is adapted from CSP

```
Configuration GasStation
    Component Customer
        Port Pay = pay!x → Pay
        Port Gas = take → pump?x → Gas
        Computation = Pay.pay!x → Gas.take → Gas.pump?x → Computation
    Component Cashier
        Port Customer1 = pay?x → Customer1
        Port Customer2 = pay?x → Customer2
        Port Topump = pump!x → Topump
        Computation = Customer1.pay?x → Topump.pump!x → Computation
            [] Customer2.pay?x → Topump.pump!x → Computation
    Component Pump
        Port Oil1 = take → pump!x → Oil1
        Port Oil2 = take → pump!x → Oil2
        Port Fromcashier = pump?x → Fromcashier
        Computation = Fromcashier.pump?x →
            (Oil1.take → Oil1.pump!x → Computation)
            [] (Oil2.take → Oil2.pump!x → Computation)
    Connector Customer_Cashier
        Role Givemoney = pay!x → Givemoney
        Role Getmoney = pay?x → Getmoney
        Glue = Givemoney.pay?x → Getmoney.pay!x → Glue
    Connector Customer_Pump
        Role Getoil = take → pump?x → Getoil
        Role Giveoil = take → pump!x → Giveoil
        Glue = Getoil.take → Giveoil.take → Giveoil.pump?x → Getoil.pump!x → Glue
    Connector Cashier_Pump
        Role Tell = pump!x → Tell
        Role Know = pump?x → Know
        Glue = Tell.pump?x → Know.pump!x → Glue
    Instances
        Customer1: Customer
        Customer2: Customer
        cashier: Cashier
        pump: Pump
        Customer1_cashier: Customer_Cashier
        Customer2_cashier: Customer_Cashier
        Customer1_pump: Customer_Pump
        Customer2_pump: Customer_Pump
        cashier_pump: Cashier_Pump
    Attachments
        Customer1.Pay as Customer1_cashier.Givemoney
        Customer1.Gas as Customer1_pump.Getoil
        Customer2.Pay as Customer2_cashier.Givemoney
        Customer2.Gas as Customer2_pump.Getoil
        casier.Customer1 as Customer1_cashier.Getmoney
        casier.Customer2 as Customer2_cashier.Getmoney
        cashier.Topump as cashier_pump.Tell
        pump.Fromcashier as cashier_pump.Know
        pump.Oil1 as Customer1_pump.Giveoil
        pump.Oil2 as Customer2_pump.Giveoil
End GasStation.
```

Figure 2: An architectural specification in WRIGHT.

[8]. Each CSP process defines an alphabet of events and the permitted patterns of events that the process may exhibit. These processes synchronize on common events (i.e., interact) when composed in parallel. WRIGHT uses such process descriptions to describe the behavior of ports, roles, computations and glues.

A *computation* specification specifies a component's behavior: the way in which it accepts certain events on certain *ports* and produces new events on those or other ports. Moreover, WRIGHT uses an overbar to distinguish initiated events from observed events *. For example, the `Customer` initiates `Pay` action (i.e., $\underline{\texttt{pay!x}}$) while the `Cashier` observes it (i.e., `pay?x`).

A *port* specification specifies the local protocol with which the component interacts with its environment through that port.

A *role* specification specifies the protocol that must be satisfied by any port that is attached to that role. Generally, a port need no have the same behavior as the role that it fills, but may choose to use only a subset of the connector capabilities. For example, the `Customer` role `Gas` and the `Customer_Pump` port `Getoil` are identical.

A *glue* specification specifies how the roles of a connector interact with each other. For example, a `Cashier_Pump` tell (Tell.pump?x) must be transmitted to the `Cashier_Pump` know ($\underline{\texttt{Know.pump!x}}$).

As a result, based on formal WRIGHT architectural

*In this paper, we use an underbar to represent an initiated event instead of an overbar that used in the original WRIGHT language definition [1].

specifications, we can infer which ports of a component are input ports and which are output ports. Also, we can infer which roles are input roles and which are output roles. Moreover, the direction in which the information transfers between ports and/or roles can also be inferred based on the formal specification. As we will show in Section 5, such kinds of information can be used to construct the information flow graph for a software architecture for computing an architectural slice efficiently.

In this paper we assume that a software architecture be represented by a formal architectural specification which contains three basic types of design entities, namely, *components* whose interfaces are defined by a set of elements called *ports*, *connectors* whose interfaces are defined by a set of elements called *roles* and the *configuration* whose topology is declared by a set of elements called *instances* and *attachments*. Moreover, each component has a special element called *computation* and each connector has a special element called *glue* as we described above.

In the rest of the paper, we assume that an architectural specification P be denoted by (C_m, C_n, c_g) where:

- C_m is the set of components in P,
- C_n is the set of connectors in P, and
- c_g is the configuration of P.

3 Motivation Example

We present a simple example to explain our approach on how to apply architectural slicing to extract reusable architectures from an existing architectural specification.

Consider the Gas Station system whose architectural representation is shown in Figure 3, and WRIGHT specification is shown in Figure 2. During the design process, suppose a system architect wants to use existing design resources to design a new system' architecture. Suppose the architect has the source code of architectural specification of the LAS system, the architect wants to reuse the source. However, instead of reusing the whole specification, the architect wishes to use only a partial specification, that is, a functionality which is concerned with the component `cashier`. A common way is to manually check the source code of the specification to find such information. However, it is very time-consuming and error-prone even for a small size specification because there may be complex dependence relations between components in the specification. If the architect has an architectural slicer at hand, the work may probably be simplified and automated without the disadvantages mentioned above. In such a scenario, an architectural slicer is invoked, which takes as input: (1) a complete architectural specification of the system, and (2) a set of ports of the component `cashier`, i.e., `Customer1`, `Customer2` and `Topump` (this is an *architectural slicing criterion*). The slicer then computes a backward and forward architectural slice respectively with respect to the criterion and outputs them to the architect. A backward architectural slice is a partial specification of the original one which includes those components and connectors that might affect the component `cashier` through the ports in the criterion, and a forward architectural slice is a partial specification of the original one which includes those components and connectors that might be affected by the component `cashier` through the ports in the criterion. The other parts of the specification that might not affect or be affected by the component `cashier` will be removed, i.e., sliced away from the original specification. The architect can thus reuse the partial architectural specification in the new system's architecture design.

4 Extraction Criteria

In this section, we give basic definitions for extracting architectural slices.

Intuitively, an *architectural slice* may be viewed as a subset of the behavior of a software architecture, similar to the original notion of the traditional static slice. However, while a traditional slice intends to isolate the behavior of a specified set of program variables, an architectural slice intends to isolate the behavior of a specified set of a component or connector's elements. Given an architectural specification $P = (C_m, C_n, c_g)$, our goal is to compute an architectural slice $S_p = (C'_m, C'_n, c'_g)$ which should be a "sub-architecture" of P and preserve partially the semantics of P. To define the meanings of the word "sub-architecture," we introduce the concepts of a reduced component, connector and configuration.

Definition 4.1 *Let $P = (C_m, C_n, c_g)$ be an architectural specification and $c_m \in C_m$, $c_n \in C_n$, and c_g be a component, connector, and configuration of P respectively:*

- *A* reduced component *of c_m is a component c'_m that is derived from c_m by removing zero, or more elements from c_m.*
- *A* reduced connector *of c_n is a connector c'_n that is derived from c_n by removing zero, or more elements from c_n.*
- *A* reduced configuration *of c_g is a configuration c'_g that is derived from c_g by removing zero, or more elements from c_g.*

The above definition showed that a reduced component, connector, or configuration of a component, connector, or configuration may equal itself in the case that none of its elements has been removed, or an *empty* component, connector, or configuration in the case that all its elements have been removed.

Having the definitions of a reduced component, connector and configuration, we can define the meaning of the word "sub-architecture".

Definition 4.2 *Let $P = (C_m, C_n, c_g)$ and $P' = (C'_m, C'_n, c'_g)$ be two architectural specifications. Then P' is a* reduced architectural specification *of P if:*

- $C'_m = \{c'_{m_1}, c'_{m_2}, \ldots, c'_{m_k}\}$ *is a "subset" of* $C_m = \{c_{m_1}, c_{m_2}, \ldots, c_{m_k}\}$ *such that for* $i = 1, 2, \ldots, k$, c'_{m_i} *is a reduced component of* c_{m_i}*,*
- $C'_n = \{c'_{n_1}, c'_{n_2}, \ldots, c'_{n_k}\}$ *is a "subset" of* $C_n = \{c_{n_1}, c_{n_2}, \ldots, c_{n_k}\}$ *such that for* $i = 1, 2, \ldots, k$, c'_{n_i} *is a reduced connector of* c_{n_i}*,*
- c'_g *is a reduced configuration of* c_g*,*

Having the definition of a reduced architectural specification, we can define some notions about slicing software architectures.

In a WRIGHT architectural specification, for example, a component's interface is defined to be a set of ports which identify the form of the component interacting with its environment, and a connector's interface is defined to be a set of roles which identify the form of the connector interacting with its environment. To understand how a component interacts with other components and connectors for extracting architectural slices, an architect must examine each port of the component of interest and each role of the connector. To satisfy these requirements, we can define a slicing criterion for a WRIGHT architectural specification as a set of ports of a component or a set of roles of a connector of interest.

Definition 4.3 *Let* $P = (C_m, C_n, c_g)$ *be an architectural specification. A* slicing criterion *for* P *is a pair* (c, E) *such that:*

1. $c \in C_m$ *and* E *is a set of elements of* c*, or*
2. $c \in C_n$ *and* E *is a set of elements of* c*.*

Note that the selection of a slicing criterion depends on architects' interests on what they want to examine. If they are interested in examining a component in an architectural specification, they may use slicing criterion 1. If they are interested in examining a connector, they may use slicing criterion 2. Moreover, the determination of the set E also depends on architects' interests on what they want to examine. If they want to examine a component, then E may be the set of ports or just a subset of ports of the component. If they want to examine a connector, then E may be the set of roles or just a subset of roles of the connector.

Definition 4.4 *Let* $P = (C_m, C_n, c_g)$ *be an architectural specification.*

- *A* backward architectural slice $S_{bp} = (C'_m, C'_n, C'_g)$ *of* P *on a given slicing criterion* (c, E) *is a reduced architectural specification of* P *which contains only those reduced components, connectors, and configuration that might directly or indirectly affect the behavior of* c *through elements in* E*.*
- Backward-slicing *an architectural specification* P *on a given slicing criterion is to find the backward architectural slice of* P *with respect to the criterion.*

Definition 4.5 *Let* $P = (C_m, C_n, c_g)$ *be an architectural specification.*

- *A* forward architectural slice $S_{fp} = (C'_m, C'_n, C'_g)$ *of* P *on a given slicing criterion* (c, E) *is a reduced architectural specification of* P *which contains only those reduced components, connectors, and configuration that might be directly or indirectly affected by the behavior of* c *through elements in* E*.*
- Forward-slicing *an architectural specification* P *on a given slicing criterion is to find the forward architectural slice of* P *with respect to the criterion.*

From Definitions 4.4 and 4.5, it is obviously that there is at least one slice of an architectural specification that is the specification itself. Moreover, the architecture represented by S_p should be a "sub-architecture" of the architecture represented by P.

Note that in contrast to define an architectural slice as a set of components, here we define an architectural slice as a reduced architectural specification of the original one that consists of either components or connectors. Our definition of an architectural slice is particularly useful for supporting architectural reuse. By using an architectural slicer, an architect can automatically decompose an existing architecture (in the case that its architectural specification is available) into some small architectures each having its own functionality which may be reused in new system designs.

5 The Information Flow Graph for Software Architectures

In this section we introduce the architecture information flow graph for software architectures on which architectural slices can be computed efficiently.

The architecture information flow graph is an arc-classified digraph whose vertices represent the ports of components and the roles of the connectors in an architectural specification, and arcs represent possible information flows between components and/or connectors in the specification.

Definition 5.1 *The* Architecture Information Flow Graph *(AIFG) of an architectural specification* P *is an arc-classified digraph* $(V_{com}, V_{con}, Com, Con, Int)$*, where* V_{com} *is the set of port vertices of* P*;* V_{con} *is the set of role vertices of* P*;* Com *is the set of component-connector flow arcs;* Con *is the set of connector-component flow arcs;* Int *is the set of internal flow arcs.*

There are three types of information flow arcs in the AIFG, namely, *component-connector flow arcs*, *connector-component flow arcs*, and *internal flow arcs*.

Component-connector flow arcs are used to represent information flows between a port of a component and a role of a connector in an architectural specification.

Connector-component flow arcs are used to represent information flows between a role of a connector and a port of a component in an architectural specification.

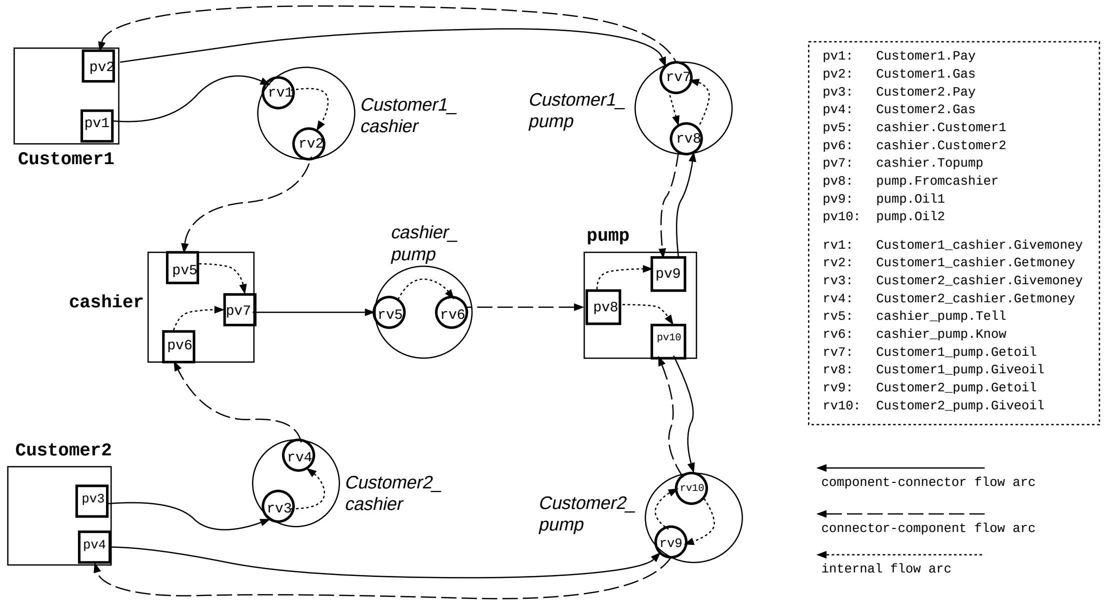

Figure 4: The information flow graph of the architectural specification in Figure 2.

Internal flow arcs are used to represent internal information flows within a component or connector in an architectural specification.

As we introduced in Section 2, Wright uses CSP-based model to specify the behavior of a component and a connector of a software architecture. Wright allows user to infer which ports of a component are input and which are output, and which roles of a connector are input and which are output based on a Wright architectural specification. Moreover, it also allows user to infer the direction in which the information transfers between ports and/or roles. As a result, by using a static analysis tool which takes an architectural specification as its input, we can construct the AIFG of a Wright architectural specification automatically.

Figure 4 shows the AIFG of the architectural specification in Figure 2. In the figure, large squares represent components in the specification, and small squares represent the ports of each component. Each port vertex has a name described by *component_name.port_name*. For example, $pv5$ (`cashier.Customer1`) is a port vertex that represents the port `Customer1` of the component `cashier`. Large circles represent connectors in the specification, and small circles represent the roles of each connector. Each role vertex has a name described by *connector_name.role_name*. For example, $rv5$ (`cashier_pump.Tell`) is a role vertex that represents the role `Tell` of the connector `cashier_pump`. The complete specification of each vertex is shown on the right side of the figure.

Solid arcs represent component-connector flow arcs that connect a port of a component to a role of a connector. Dashed arcs represent connector-component flow arcs that connect a role of a connector to a port of a component. Dotted arcs represent internal flow arcs that connect two ports within a component (from an input port to an output port), or two roles within a connector (from an input role to an output role). For example, $(rv2, pv5)$ and $(rv6, pv8)$ are connector-component flow arcs. $(pv7, rv5)$ and $(pv9, rv8)$ are component-connector flow arcs. $(rv1, rv2)$ and $(pv8, pv10)$ are internal flow arcs.

6 Extracting Reusable Architectures

Roughly speaking, the process of extracting reusable architectures is how to find some architectural slices defined in this paper. However, the slicing notions defined in Section 4 give us only a general view of an architectural slice, and do not tell us how to compute it. In [21] we presented a two-phase algorithm to compute a slice of an architectural specification based on its information flow graph. Our algorithm contains two phases: (1) Computing a slice S_g over the information flow graph of an architectural specification, and (2) Constructing an architectural slice S_p from S_g.

6.1 Computing a Slice over the AIFG

Let $P = (C_m, C_n, c_g)$ be an architectural specification and $G = (V_{com}, V_{con}, Com, Con, Int)$ be the AIFG of P. To compute a slice over the G, we refine the slicing notions defined in Section 4 as follows:

- *A slicing criterion for G is a pair (c, V_c) such that: (1) $c \in C_m$ and V_c is a set of port vertices corresponding to the ports of c, or (2) $c \in C_n$ and V_c is a set of role vertices corresponding to roles of c.*

- *The slice $S_{bg}(c, V_c)$ of G on a given slicing criterion (c, V_c) is a subset of vertices of G such that for any*

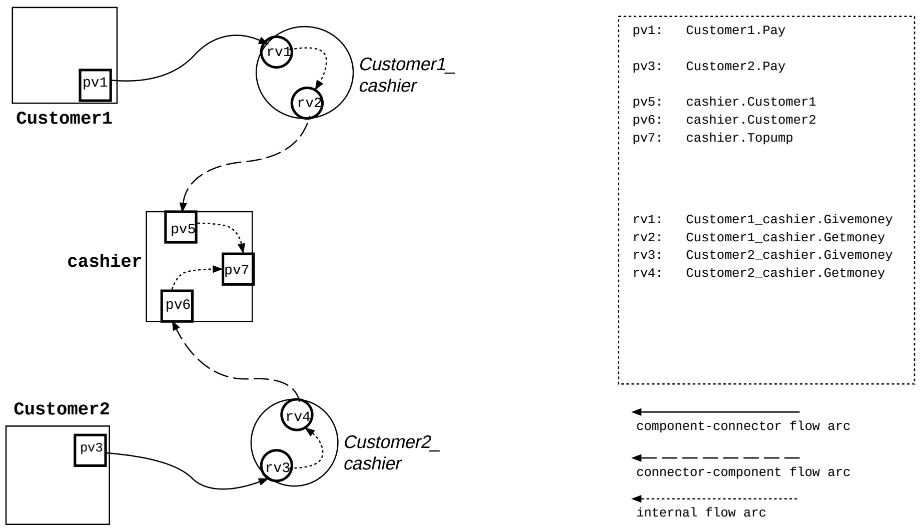

Figure 5: A slice over the AIFG of the architectural specification in Figure 2.

vertex v of G, $v \in S_{bg}(c, V_c)$ iff there exists a path from v to $v' \in V_c$ in the AIFG.

According to the above descriptions, the computation of a slice over the AIFG can be solved by using an usual depth-first or breath-first graph traversal algorithm to traverse the graph by taking some port or role vertices of interest as the start point of interest.

Figure 5 shows a slice over the AIFG with respect to the slicing criterion $(\texttt{cashier}, V_c)$ such that $V_c = \{pv5, pv6, pv7\}$.

6.2 Computing an Architectural Slice

The slice S_g computed above is only a slice over the AIFG of an architectural specification, which is a set of vertices of the AIFG. Therefore we should map each element in S_g to the source code of the specification. Let $P = (C_m, C_n, c_g)$ be an architectural specification and $G = (V_{com}, V_{con}, Com, Con, Int)$ be the AIFG of P. By using the concepts of a reduced component, connector, and configuration introduced in Section 4, a slice $S_p = (C'_m, C'_n, c'_g)$ of an architectural specification P can be constructed in the following steps:

1. Constructing a reduced component c'_m from a component c_m by removing all ports such that their corresponding port vertices in G have not been included in S_g and unnecessary elements in the computation from c_m. The reduced components C'_m in S_p have the same relative order as the components C_m in P.

2. Constructing a reduced connector c'_n from a connector c_n by removing all roles such that their corresponding role vertices in G have not been included in S_g and unnecessary elements in the glue from c_n. The reduced connectors C'_n in S_p have the same relative order as their corresponding connectors in P.

3. Constructing the reduced configuration c'_g from the configuration c_g by the following steps:

   – Removing all component and connector instances from c_g that are not included in C'_m and C'_n.

   – Removing all attachments from c_g such that there exists no two vertices v_1 and v_2 where $v_1, v_2 \in S_g$ and `v1 as v2` represents an attachment.

   – The instances and attachments in the reduced configuration in S_p have the same relative order as their corresponding instances and attachments in P.

Figure 6 shows a slice of the WRIGHT specification in Figure 2 with respect to the slicing criterion (`cashier`, E) such that E={`Customer1`, `Customer2`, `Topump`} is a set of ports of component `cashier`. The small rectangles represent the parts of specification that have been removed, i.e., sliced away from the original specification. The slice is obtained from a slice over the AIFG in Figure 5 according to the mapping process described above.

7 Concluding Remarks

In this paper, we applied architectural slicing to extract reusable architectures from existing architectural specifications. Abstractly, our architectural slicing algorithm takes as input a formal architectural specification (written in its associated architectural description language) of a software system, then it removes from the specification those components and interconnections between

```
Configuration GasStation
    Component Customer
        Port Pay = pay!x → Pay
        □□□□□□□□□□□□□□□□□□□□□□
        Computation = Pay.pay!x → Gas.take → Gas.pump?x → Computation
    Component Cashier
        Port Customer1 = pay?x → Customer1
        Port Customer2 = pay?x → Customer2
        Port Topump = pump!x → Topump
        Computation = Customer1.pay?x → Topump.pump!x → Computation
            [] Customer2.pay?x → Topump.pump!x → Computation
    □□□□□□□□□□□□□□□□□
        □□□□□□□□□□□□□□□□□□□□□□
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    Connector Customer_Cashier
        Role Givemoney = pay!x → Givemoney
        Role Getmoney = pay?x → Getmoney
        Glue = Givemoney.pay?x → Getmoney.pay!x → Glue
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    Instances
        Customer1: Customer
        Customer2: Customer
        cashier: Cashier
        □□□□□□□□
        Customer1_cashier: Customer_Cashier
        Customer2_cashier: Customer_Cashier
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    Attachments
        Customer1.Pay as Customer1_cashier.Givemoney
        □□□□□□□□□□□□□□□□□□□□□□□□□□□
        Customer2.Pay as Customer2_cashier.Givemoney
        □□□□□□□□□□□□□□□□□□□□□□□□□□□
        casier.Customer1 as Customer1_cashier.Getmoney
        casier.Customer2 as Customer2_cashier.Getmoney
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    End GasStation.
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Figure 6: A backward slice of the architectural specification in Figure 2.

components which are not interested by the architect. The rest of the specification, i.e., its architectural slice, can thus be used by the architect in a new system architecture design. This benefit allows one to rapidly reuse existing architecture design resources when performed architecture design.

While our initial exploration used Wright as the architecture description language, the concept and approach are language-independent. However, the implementation of an architectural slicing tool may differ from one architecture description language to another because each language has its own structure and syntax which must be handled carefully.

To demonstrate the usefulness of our slicing approach, we are implementing a slicer for Wright architectural descriptions to support architectural-level understanding and reuse.

References

[1] R. Allen, "A Formal Approach to Software Architecture," PhD thesis, Department of Computer Science, Carnegie Mellon University, 1997.

[2] J. Beck and D. Eichmann, "Program and Interface Slicing for Reverse Engineering," *Proceeding of the 15th International Conference on Software Engineering*, pp.509-518, Baltimore, Maryland, IEEE Computer Society Press, 1993.

[3] G. Canfora, A. Cimitile, A. De Lucia, and G. A. Di Lucca, "Software Salvaging Based on Conditions," *Proceedings of the International Conference on Software Maintenance*, pp.424-433, Victoria, Canada, September 1994.

[4] A. De Lucia, A. R. Fasolino, and M. Munro, "Understanding function behaviors through program

slicing," *Proceedings of the Fourth Workshop on Program Comprehension*, Berlin, Germany, March 1996.

[5] J.Ferrante, K.J.Ottenstein, and J.D.Warren, "The Program Dependence Graph and Its Use in Optimization," *ACM Transaction on Programming Language and System*, Vol.9, No.3, pp.319-349, 1987.

[6] K. B. Gallagher and J. R. Lyle, "Using Program Slicing in Software Maintenance," *IEEE Transaction on Software Engineering*, Vol.17, No.8, pp.751-761, 1991.

[7] D. Garlan, R. Monroe, and D. Wile, "ACME: An Architecture Description Interchange Language," *Proceedings of CASCON'97*, November 1997.

[8] C.A.R. Hoare, "Communicating Sequential Processes," Prentice Hall, 1985.

[9] D. Helmbold and D. Luckham, "Debugging Ada Tasking Programs," *IEEE Software*, Vol.2, No.2, pp.47-57, 1985.

[10] S. Horwitz, T. Reps, and D. Binkley, "Interprocedural Slicing Using Dependence Graphs," *ACM Transaction on Programming Language and System*, Vol.12, No.1, pp.26-60, 1990.

[11] F. Lanubile and G. Visaggio, "Extracting Reusable Functions By Flow Graph-Based Program Slicing," *IEEE Transaction on Software Engineering*, Vol.23, No.4, pp.246-259, April 1997.

[12] D. C. Luckham, L. M. Augustin, J. J. Kenney, J. Veera, D. Bryan, and W. Mann, "Specification Analysis of System Architecture Using Rapide," *IEEE Transaction on Software Engineering*, Vol.21, No.4, pp.336-355, April 1995.

[13] R. T. Monroe and D. Garlan, "Style-Based Reuse for Software Architectures," *Proc. 4th International Conference on Software Reuse*, pp., 1996.

[14] G. Naumovich, G.S. Avrunin, L.A. Clarke, and L.J.Osterweil, "Applying Static Analysis to Software Architectures," *Proceedings of the Sixth European Software Engineering Conference*, LNCS, Vol.1301, pp.77-93, Springer-Verlag, 1997.

[15] K. J. Ottenstein and L. M. Ottenstein, "The Program Dependence Graph in a software Development Environment," *ACM Software Engineering Notes*, Vol.9, No.3, pp.177-184, 1984.

[16] M. Shaw, R. DeLine, D. V. Klein, T. L. Ross, D. M. Young, and G. Zelesnik, "Abstractions for Software Architecture and Tools to Support Them," *IEEE Transaction on Software Engineering*, Vol.21, No.4, pp.314-335, April 1995.

[17] M. Shaw and D. Garlan, "Software Architecture: Perspective on an Emerging Discipline," Prentice Hall, 1996.

[18] F. Tip, "A Survey of Program Slicing Techniques," *Journal of Programming Languages*, Vol.3, No.3, pp.121-189, September, 1995.

[19] M. Weiser, "Program Slices: Formal, Psychological, and Practical Investigations of an Automatic Program Abstraction Method," PhD thesis, University of Michigan, Ann Arbor, 1979.

[20] J. Zhao, "Using Dependence Analysis to Support Software Architecture Understanding," in M. Li (Ed.), *New Technologies on Computer Software*, pp.135-142, International Academic Publishers, September 1997.

[21] J. Zhao, "Applying Slicing Technique to Software Architectures," *Proc. Fourth IEEE International Conference on Engineering of Complex Computer Systems*, pp.87-98, August 1998.